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10/816,451	03/31/2004	Anthony L. Chun	1020.P18418	9245

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	PAPER NUMBER
2181	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,451	CHUN ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4 and 15-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Fette et al., U.S. Patent No. 4,862,407 (Hereinafter Fette).

3. Referring to claim 1, Fette has taught an apparatus, comprising:

a memory unit *[dual port memory; Fig. 1, component 19]* to store input data for a plurality of functions *[column 4, line 64 – column 5, line 2]*;

a control unit *[microsequencer; Fig. 2, component 27]* to control execution of said plurality of functions *[column 5, lines 63-65]*, said control unit having a trigger queue *[function register; Fig. 3, component 80]* to store function identifiers *[column 8, lines 8-13]*, said control unit to select a function to execute using a function identifier from said trigger queue *[column 7, lines 15-22]*; and

a plurality of execution units operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier *[column 5, line 63 – column 6, line 7]*; and

trigger logic *[host processor 11 and dual port memory element 19]* to determine when a sufficient amount of input data for a function has been stored in said memory unit *[the host processor communicates with coprocessor 20 after writing a function block to memory (i.e. after determining when a sufficient amount of input data has been stored); column 4, line 64 – column 5, line 2]*, and send a triggered function identifier to said control unit when a sufficient amount of input data for a function has been stored in said memory unit *[column 7, lines 15-22]*.

4. Referring to claim 3, Fette has taught the apparatus of claim 1, wherein said trigger logic sends a trigger write signal *[begin signal]* to said control unit with said triggered function identifier *[column 7, lines 3-14]*.

5. Referring to claim 4, Fette has taught the apparatus of claim 3, wherein said control unit receives said triggered function identifier and trigger write signal, and writes said triggered function identifier in said trigger queue *[the microsequencer receives the begin signal (column 7, lines 3-14) and receives a function input (column 7, lines 15-22), which is written to function register 80 (column 8, lines 8-13)]*.

6. Referring to claim 15, Fette has taught a method, comprising:

receiving a first signal indicating input data for a function has been received *[the host processor determines when a sufficient amount of input data has been stored; column 4, line 64 – column 5, line 2]*;

sending a triggered function identifier and trigger write signal to a trigger queue when a sufficient amount of input data for a function has been stored in a memory unit *[the host processor sends a begin signal (trigger write signal) (column 7, lines 3-14) and the memory outputs function input (column 7, lines 15-22)]*;

receiving said triggered function identifier and trigger write signal at said trigger queue *[the microsequencer receives the begin signal (column 7, lines 3-14) and receives a function input (column 7, lines 15-22)]*; and

writing said triggered function identifier in said trigger queue in response to said trigger write signal *[the function input is written to function register 80; column 8, lines 8-13]*.

7. Referring to claim 16, Fette has taught the method of claim 15, further comprising: receiving a trigger read signal at said trigger queue; and sending a function identifier for a function to a control unit in response to said trigger read signal *[column 8, lines 8-29]*.

8. Referring to claim 17, Fette has taught the method of claim 16, further comprising: receiving said function identifier for a function from said trigger queue; generating a reconfigurator vector using said function identifier; sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector; and sending function control signals to a plurality of execution units to process said input data in accordance with said reconfigurator vector *[column 6, lines 14-31]*.

9. Referring to claim 18, Fette has taught the method of claim 17, wherein said generating comprises: receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and register status values from said execution units, at said control unit state machine *[column 7, lines 31-38]*; generating an operation number address using said inputs; converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[column 8, lines 8-13]*.

10. Referring to claim 19, Fette has taught an article comprising:

a storage medium *[host memory; column 3, lines 58-65]*;

said storage medium including stored instructions that, when executed by a processor, result in receiving a first signal indicating input data for a function has been received *[the host processor determines when a sufficient amount of input data has been stored; column 4, line 64 – column 5, line 2]*, sending a triggered function identifier and trigger write signal to a trigger queue when a sufficient amount of input data for a function has been stored in a memory unit *[the host processor sends a begin signal (trigger write signal) (column 7, lines 3-14) and the memory outputs function input (column 7, lines 15-22)]*, receiving said triggered function identifier and trigger write signal at said trigger queue *[the microsequencer receives the begin signal (column 7, lines 3-14) and receives a function input (column 7, lines 15-22)]*, and writing said triggered function identifier in said trigger queue in response to said trigger write signal *[the function input is written to function register 80; column 8, lines 8-13]*.

11. Referring to claim 20, Fette has taught the article of claim 19, wherein the stored instructions, when executed by a processor, further result in receiving a trigger read signal at said trigger queue, and sending a function identifier for a function to a control unit in response to said trigger read signal *[column 8, lines 8-29]*.

12. Referring to claim 21, Fette has taught the article of claim 20, wherein the stored instructions, when executed by a processor, further result in receiving said function identifier for a function from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector,

and sending function control signals to a plurality of execution units to process said input data in accordance with said reconfigurator vector *[column 6, lines 14-31]*.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fette in view of Crabill, U.S. Patent No. 6,725,364.

15. Referring to claim 5, Fette has taught the apparatus of claim 4, wherein said control unit comprises: a control unit state machine module *[microcode ROM; Fig. 3, component 82]*, said control unit state machine to output an operation number address; and a control unit lookup table to be configured with table content data, said control unit lookup table to convert said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[column 8, lines 8-29]*.

Fette has not explicitly taught that the control unit state machine module is to be configured in accordance with a fuse map.

Crabill has taught using configuration parameters to reprogram field programmable gate array microcode storage *[column 3, lines 46-50]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the apparatus of Fette to comprise a reprogrammable field programmable gate array microcode storage that is configured in accordance with configuration parameters. In the case of field programmable gate arrays, the configuration parameters inherently include a fuse map.

The motivation for doing so would have been that the apparatus would be more flexible *[Crabill; column 1, lines 60-66]*.

16. Referring to claim 6, Fette and Crabill have taught the apparatus of claim 5, wherein said trigger queue receives a trigger read signal as input, said trigger queue to send said function identifier to said control state machine module in response to said trigger read signal *[Fette; column 8, lines 8-29]*.

17. Referring to claim 7, Fette and Crabill have taught the apparatus of claim 6, wherein said control unit further comprises: an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal *[Fette; column 7, lines 31-38]*; an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal *[Fette; column 7, lines 31-38]*; and a register file module to store a state for one function while another function is being executed by said execution units *[Fette; column 8, lines 8-13]*

18. Referring to claim 8, Fette and Crabill have taught the apparatus of claim 7, wherein said control unit state machine module receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state index value, and register status values from said execution units, and uses said inputs to generate said operation number address *[Fette; column 8, lines 8-29]*.

19. Claims 9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fette in view of the examiner taking of Official Notice.

20. Referring to claim 9, Fette has taught a system, comprising:

a host processing system *[host processor; Fig. 1, component 11]*; and

a reconfigurable communication architecture module having a filter micro-code accelerator processing engine, said processing engine comprising:

a memory unit *[dual port memory; Fig. 1, component 19]* to store input data for a plurality of functions *[column 4, line 64 – column 5, line 2]*;

a control unit *[microsequencer; Fig. 2, component 27]* to control execution of said plurality of functions *[column 5, lines 63-65]*, said control unit having a trigger queue *[function register; Fig.*

3, component 80] to store function identifiers *[column 8, lines 8-13]*, said control unit to select a function to execute using a function identifier from said trigger queue *[column 7, lines 15-22]*; and

a plurality of execution units operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier *[column 5, line 63 – column 6, line 7]*; and

trigger logic *[host processor 11 and dual port memory element 19]* to determine when a sufficient amount of input data for a function has been stored in said memory unit *[the host processor communicates with coprocessor 20 after writing a function block to memory (i.e. after determining when a sufficient amount of input data has been stored); column 4, line 64 – column 5, line 2]*, and send a triggered function identifier to said control unit when a sufficient amount of input data for a function has been stored in said memory unit *[column 7, lines 15-22]*.

Fette has not explicitly taught that the digital signal processing system includes an antenna.

However, Examiner takes Official Notice that including an antenna in a digital signal processing system is well-known and conventional.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Fette to include an antenna since doing so would allow the system to advantageously support wireless communication applications.

21. Referring to claim 11, Fette has taught the system of claim 9, wherein said trigger logic sends a trigger write signal *[Fette; begin signal]* to said control unit with said triggered function identifier *[Fette; column 7, lines 3-14]*.

22. Referring to claim 12, Fette has taught the system of claim 11, wherein said control unit receives said triggered function identifier and trigger write signal, and writes said triggered function identifier in said trigger queue *[Fette; the microsequencer receives the begin signal (column 7, lines 3-14) and receives a function input (column 7, lines 15-22), which is written to function register 80 (column 8, lines 8-13)]*.

23. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fette in view of the examiner's taking of Official Notice, and further in view of Crabill.

24. Referring to claim 13, Fette has taught the system of claim 12, wherein said control unit comprises: a control unit state machine module *[Fette; microcode ROM; Fig. 3, component 82]*, said control unit state machine to output an operation number address; and a control unit lookup table to be configured with table content data, said control unit lookup table to convert said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[Fette; column 8, lines 8-29]*.

Fette has not explicitly taught that the control unit state machine module is to be configured in accordance with a fuse map.

Crabill has taught using configuration parameters to reprogram field programmable gate array microcode storage *[column 3, lines 46-50]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Fette to comprise a reprogrammable field programmable gate array microcode storage that is configured in accordance with configuration parameters. In the case of field programmable gate arrays, the configuration parameters inherently include a fuse map.

The motivation for doing so would have been that the apparatus would be more flexible *[Crabill; column 1, lines 60-66]*.

25. Referring to claim 14, Fette and Crabill have taught the system of claim 13, wherein said trigger queue receives a trigger read signal as input, said trigger queue to send said function identifier to said control state machine module in response to said trigger read signal *[Fette; column 8, lines 8-29]*.

Response to Arguments

26. Applicant's arguments filed 02/23/2009 have been fully considered but they are not persuasive.

27. Applicant argues that novelty/rejection of the claims, in substance that:

A) "[T]he host processor and dual port memory of Fette do not comprise trigger logic to determine when a sufficient amount of input data for a function has been stored in said memory unit, and to send a triggered function identifier to said control unit when sufficient amount of input data for a function has been stored in said memory unit, as recited in amended independent claim 1." (page 10 of remarks)

B) "Applicant respectfully submits that the limitations in the above recited claims, asserted to be well-known, or to be common knowledge in the art, are not capable of instant and unquestionable demonstration as being well-known." (page 13 of remarks)

C) "Applicant respectfully submits that the Office Action fails, however, to provide a factual basis that proves the only way to configure a control state machine module in accordance with a fuse map is using an FPGA." (page 13 of remarks)

28. These arguments are not found persuasive for the following reasons.

29. Regarding point A), Fette has taught that the host processor communicates with coprocessor 20 after writing a function block to memory. See column 4, line 64 – column 5, line 2. That is, the host processor determines whether a complete function block has been written (i.e. whether a sufficient amount of input data has been stored) before communicating with the coprocessor. This communication includes a triggered function identifier because the communication results in triggering the execution of a particular function. See column 7, lines 15-22. Therefore, Fette has taught trigger logic to determine when a sufficient amount of input data for a function has been stored in said memory unit, and to send a triggered function identifier to said control unit when sufficient amount of input data for a function has been stored in said memory unit as recited in the claims.

30. Regarding point B), the examiner directs Applicant's attention to Verbauwhede et al., "Low Power DSP's for Wireless Communications" which describes digital signal processors in the context of wireless communications applications. See Abstract. As indicated in Fig. 2, an antenna is typically used in wireless communications. Therefore, as indicated in the rejection of the claims, antennas are well-known in digital signal processing systems.

31. Regarding point C), the examiner notes that, contrary to Applicant's statement, the examiner has not indicated that "the only way to configure a control state machine module in accordance with a fuse map is using an FPGA." Instead the examiner has indicated that it would have been obvious to modify the system of Fette to comprise a reprogrammable field programmable gate array (FPGA) microcode

storage that is configured in accordance with configuration parameters as taught by Crabill and that, in the case of FPGAs, the configuration parameters inherently include a fuse map.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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